PATENT
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P. Walker
8-29-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of)
)
Inventor: Vladislav Vashchenko, et al.)
)
Serial No.: 09/816,287)
)
Filed: March 21, 2001)
)
Title: HIGH HOLDING VOLTAGE ESD)
)
PROTECTION STRUCTURE AND METHOD)
)

PRELIMINARY AMENDMENT

This communication is a preliminary amendment to the above-referenced application.

Please make the following clerical error:

On page 11, line 17, replace the "□" symbols with "μ" symbol. The dimensions in the μm range are typical of current technology as appears from Figure 5, and would have been clear to a person skilled in the art The correction therefore adds no new subject matter and it is respectfully requested that the changes be entered.

For purposes of convenience, the replacement page of the changes are included.

Respectfully Submitted,

Dated: 4/12, 2001

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injected into material 310 from n+ (npn emitter) region 322. Thus, when the number of holes flowing into material 310 decreases, relative to the electrons injected into material 310 from n+ region 322 the space change is neutralized to a lesser extent thereby increasing the holding voltage of device 300. Thus, by properly sizing the p-emitter 316, the magnitude of the holding voltage of device 300 can be increased above a dc bias that is present on the to-be-protected node. As a result, device 300 turns off following an ESD event. In another embodiment, the p+ emitter is reduced in size to below a critical size, and the space charge neutrality adjusted by appropriately increasing the n+ emitter.

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FIG. 5 shows a graphical representation that illustrates the V-I characteristics of the device of the present invention for various sizes of the p+ region316. The evaluation was for a human-body model (HBM) ESD pulse using a thermally-coupled mixed-mode device simulation.) As shown in FIG. 5, decreasing the p+ emitter increases the holding voltage of the device after snapback. Thus, one advantage of the invention is that it provides an ESD protection device, the current density and holding voltage characteristics of which can be selected to lie anywhere between those offered by GGNMOS and regular LVTSCR devices. In fact, as shown in Figure 6, one embodiment of the device of the invention, which used a n-well 312 depth of 1.2μm, a p+ emitter depth of 1μm, and a n+ region 314 depth of 2.5μm delivered three times higher current in the on-state (graph 62) than a GGNMOS device (graph 64). Thus, the device of the invention provides an ESD protection solution which either allows a significant decrease in physical size of the device over a GGNMOS or protects against at least three times higher ESD pulse amplitudes for a given contact width while providing essentially the same holding voltage.

It should be understood that various alternatives to the embodiments of the invention described herein may be employed in practicing the invention to achieve varying amounts of holes being injected compared to electrons. It will also be appreciated that the structure can be formed with opposite polarity elements so that, instead of holes, the minority carriers are electrons. In such an embodiment, the n+ emitter formed in a p+ well would be reduced in size to limit the injection of the electrons relative to holes. Thus, it is intended that the following claims define the scope of the invention and that methods and structures within the scope of these claims and their equivalents be covered thereby.